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DESIGN AND DEVELOPMENT OF A HIGH POWER, LOW SATURATION VOLTAGE SILICON SWITCHING TRANSISTOR

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I. INTRODUCTION

Theoretical considerations and past experience indicate the feasibility of developing a transistor with a saturation voltage of 0.1 volt at 75A collector current. This is the object of the present effort, with a design goal of 0.07V.

The methods employed in this effort include designing the surface geometry in order to operate the transistor at as low a current density as possible, and to employ an internal structure which affords the greatest possible symmetry in the emitter-base and collector-base junctions.

The use of commercially available thin crystal seems to be a logical extension of the presently successfuly simultaneously diffused process as another alternative. This material should permit steeper concentration gradients, thereby increasing injection efficiencies as well as reducing series resistance in the emitter and collector regions. While high rates of breakage were anticipated, additional problems of uniformity and difficulties in mounting have cast doubt on the production feasibility of this approach.

Control of the collector geometry is being investigated by both epitaxial and symmetrically diffused techniques. Progress on all of these approaches is described in the following section.

II. PROGRESS DURING THE CURRENT QUARTER

A. THIN-WAFER APPROACH

Reasonable yields of thin wafers have been achieved through the emitter-collector drive-in diffusion. This was achieved by mounting the wafers on aluminum-carrier discs through photoresist processes and careful handling techniques. Material cut to the final diameter by the supplier has been received and has alleviated the problem of breakage while cutting wafers to size.

Continued processing on thin wafers has revealed some difficulties not originally anticipated. The hard-soldering technique used for wafers of conventional thickness (5-6 mils) has been found to be completely unsatisfactory for thin wafers. The soldering material was found to alloy through the total thickness of the 2.5 mil wafer. Clear evidence of this is shown in the photograph in Figure 1. Since this hard-soldering process has been found essential to the successful fabrication of very large devices, a suitable modification of this process must be found if the thin-wafer approach is to be continued.

A second observation which may prove to be a problem is the fact that commercially available thin wafers have rather rough back surfaces. While these surfaces have been etched to remove work damage, the resulting surface is probably too rough to provide the uniformity considered necessary for junction voltages to cancel out and provide low $V_{CE(sat)}$. This roughness is shown in a bevelled thin-wafer device shown in Figure 2. Smaller transistors which can be encapsulated without the previously mentioned difficulties are currently being fabricated in order to determine whether this roughness is detrimental and whether the thin-wafer approach in general offers a significant advantage.

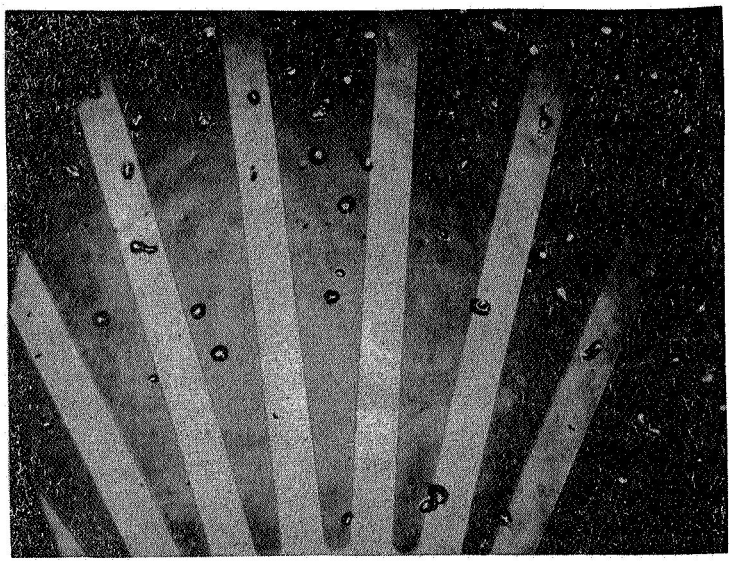


Figure 1. Surface of Thin Wafer Transistor After Molybdenium Mounting (15x)

A third difficulty is that parallelism is not always sufficient for the fabrication of simultaneously diffused transistors. On one simultaneously diffused thin-wafer sample, the base width was found to taper from 8 microns in one position to complete puncture over a distance of only 5 mm. (NOTE: The apparent taper of the base width in the sample in Figure 2 is largely an artifact of imperfect bevelling, and it is not to be considered an example of the above observation.)

B. EPITAXIAL APPROACH

The first attempt at epitaxial selective collector utilized an arsenic diffusion into a .01 ohm-cm, N-type substrate, then the P-type epitaxial base layer was grown over this structure. The height of the collector step in this run was only 0.15 μ. In order to make this step more pronounced, the second run utilized a thin N-type epitaxial layer (4 μ thick, 11 ohm-cm), then arsenic was diffused selectively into this layer, and finally the P-type base layer was grown over this structure. Data are not yet available for these runs.

C. SYMMETRICALLY DIFFUSED APPROACH

The greatest amount of effort has been placed on the symmetrically diffused approach. Equipment required to implement the selective collector has been received and is now operational. As mentioned in the first quarterly report, this process requires a photoresist alignment machine which permits the placing of aligned geometries on opposite sides of the wafer. The machine has two special capabilities to allow this. First, two masks may be aligned with respect to each other; then a wafer which has been coated with KMER on both sides is sandwiched between the masks, and both sides are exposed simultaneously. This method provides good registration of the two images, but alignment of the pattern with respect to the edges of the silicon wafer is rather coarse since this must be done strictly by hand. The second special

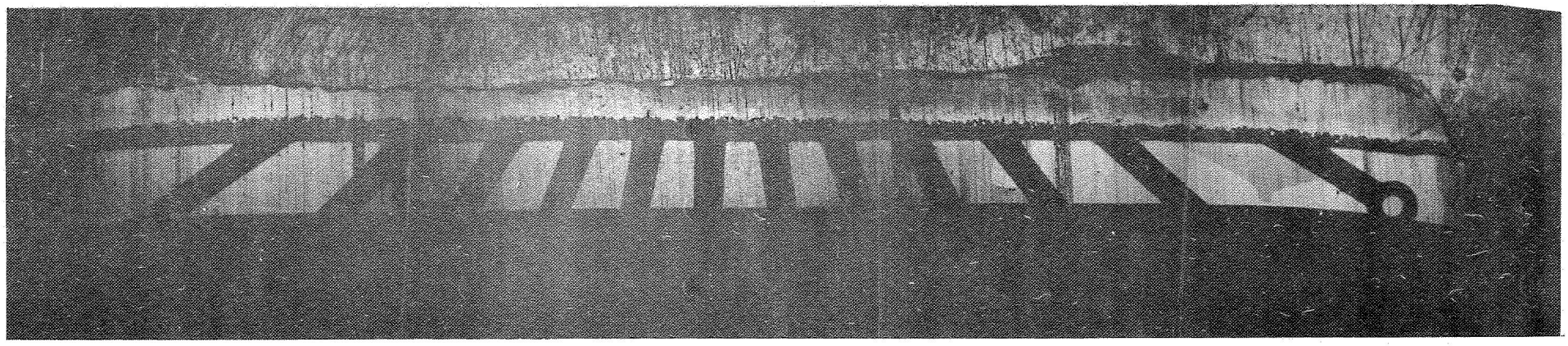


Figure 2. Bevelled Cross Section of Thin Wafer Transistor Showing Ragged Collector

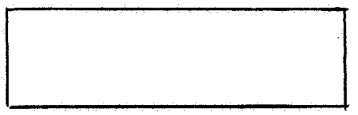
capability of the machine is to perform alignments with infrared light transmitted through the slice. This permits alignment to metal patterns on heavily diffused areas on the opposite side of the slice.

The special capabilities of the alignment machine have been used in the following ways.

1. After the N^+ deposit the double-sided-exposure capability is used to etch patterns in the silicon on both sides of the wafer. The subsequent process steps include an N^+ drive, collector lapping, N^+ deposit on the collector side of the slice, and another drive. The complete process flow was described in the first quarterly report.

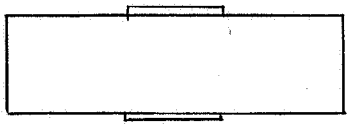
2. The material is initially oxidized, then the double-sided-exposure capability is used to etch matched patterns in the oxide on both sides of the wafer. The N^+ deposit is now performed, and penetrates the oxide; however, the deposit in the unmasked areas penetrates deeper and achieves a higher concentration. Now it is necessary to etch away the shallow N-layer in the base contact regions. Since the silicon has a rough (lapped) surface, the pattern is nearly invisible. The infrared transmission feature of the alignment machine has been useful in aligning a mask to the heavily phosphorous-diffused areas. This process requires no collector lapping step or any additional phosphorous deposit and drive steps. The use of wafers which are polished on the front side would simplify this process since the emitter mask could be aligned to the step on the surface which always occurs during diffusion in an oxidizing atmosphere, and the use of infrared would not be required. The flow for this process is shown in Figure 3.

Figure 3. Symmetrically Diffused Transistor
Oxide Process

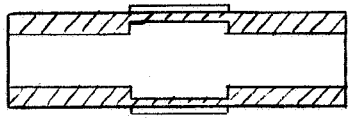


Starting Material
20 Ohm-cm P-Type
5-6 mils Thick

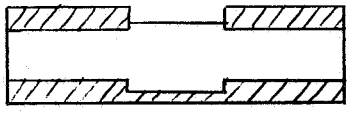
Oxidation
10,000 - 12,000 Å Thick



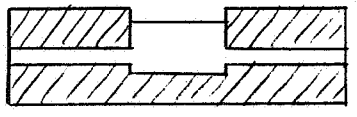
Emitter-Collector Masking
Define Emitter and Collector
Geometries in Oxide



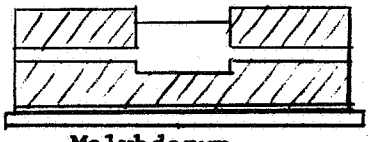
N^+ Deposit
x_j = 5-6 μ
ρ_s = 1 ohm-cm/□



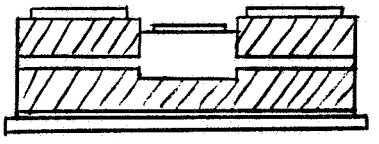
Emitter Masking
Etch Away Shallow N-Layer



N^+ Drive
W_B = 10-12 μ



Molybdenum Mounting
Ag Solder



Contact Evaporation
Al 30 KÅ

Data from units made by this process are shown in Table 1. The difference between the selective collector units and the non-selective collector control unit is not clear. This may be due to the rather small collector step height, or simply to the small sample which is not statistically adequate. All of the saturation voltage data in this report were measured on a pulsed gain tester as a laboratory reference. More specific data will be acquired when they can be measured on the precision DC tester.

Units utilizing the lapped collector method suffered from high breakage losses. Furthermore, the units which survived to the moly mount step appeared to have collector-base shorts. In light of the observation on alloying through thin wafers, it is reasonable to assume that the alloying penetrated the thin parts of the collector. Future attempts at this process should use a shorter initial drive with the final base width being achieved in the second drive. This will permit penetration of the shallower parts of the collector to a depth which should not be affected by the moly mount process.

Other improvements in addition to the basic lines of investigation are being implemented. It was mentioned in the first quarterly report that the sunburst geometry had been redesigned for increased emitter edge length. Photoresist masks have been received and are being evaluated. Table 2 presents data comparing the performance of the new geometry with the currently used design. The units with the new geometry were encapsulated with parts designed for the older geometry. This practice will be continued unless it becomes evident that larger emitter and base contacts will produce a significant improvement in saturation voltage.

Comparison data are presented in Table 2. The effect of the increased emitter edge length is not obvious, but again the sample size is not statistically adequate. However, it is significant to observe that the saturation voltages are very close to objectives. As the processes become established, more samples will be evaluated.

In the emitter drive step for symmetrically diffused transistors, it is necessary to perform the drive in a boron atmosphere in order to prevent the redistribution of phosphorous from the emitter areas into the base contact areas, converting those areas to N-type. Boron trioxide (B_2O_3), usually used to provide the boron atmosphere, has been found to be somewhat unreliable in performing this function. Variations in flow rates of the gases and temperature of the source zone can greatly affect the B_2O_3. In order to improve this situation, a boron tribromide (BBr_3) doping system has been installed on the drive furnace. In addition to providing reliable compensation of the redistributed phosphorous, the system provides a much higher concentration P^+ layer in the base contact areas. The resulting reduction of the base resistance should decrease $V_{BE(sat)}$ with a corresponding reduction of $V_{CE(sat)}$.

IV. PROGRAM FOR THE NEXT PERIOD

Refinement of processes will be continued, and more test samples will be fabricated and evaluated.

Table 1

Unit No.	Description	h_{FE}	I_C	V_{CE}	$V_{CE(sat)}$	$V_{CE(sat)}$	I_C	I_B
JS-102A-1	Non-Selective Collector	25	75A	1V	0.1V	.88V	75A	5A
JS-102B-1	Selective Collector	30	75A	1V	0.15V	.9V	75A	5A
JS-102B-2	Selective Collector	50	75A	1V	0.1V	.85V	75A	5A

Table 2

Unit No.	Descritpion	h_{FE}	I_C	V_{CE}	$V_{CE(sat)}$	$V_{CE(sat)}$	I_C	I_B
JS-105A-1	Older Geometry 18" Emitter Edge	23	75A	1V	.1V	.9V	75A	10A
JS-105A-2	Older Geometry 18" Emitter Edge	31	75A	1v	.1V	.85V	75A	5A
JS-105A-3	Older Geometry 18" Emitter Edge	25	75A	1V	.1V	.88V	75A	10A
JS-105A-4	Older Geometry 18" Emitter Edge	21	75A	1V	.1V	.94V	75A	10A
JS-105B-1	New Geometry 23" Emitter Edge	20	75A	1V	.08V	.85V	75A	10A
JS-105B-2	New Geometry 23" Emitter Edge	27	75A	1V	.1V	.84V	75A	5A
JS-105B-3	New Geometry 23" Emitter Edge	12.5	75A	1V	.1V	.85V	75A	10A
JS-105B-4	New Geometry 23" Emitter Edge	11.5	75A	1V	.15V	.88V	75A	10A